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10EC/TE71

Seventh Semester B.E. Degree Examination, June/July 2014
Computer Communication Networks

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Describe the layer presentation in the TCP/IP model and explain the protocol of each layer. **(08 Marks)**

b. What is ADSL? Explain the operation of ADSL using discrete multi tone modulation with a neat diagram. **(08 Marks)**

c. List diagram types of addressing. Explain any one type of addressing with suitable examples. **(04 Marks)**

2 a. What is framing? Explain bit stuffing with a help of a diagram. **(05 Marks)**

b. With neat diagram, explain HDLC frame format. **(05 Marks)**

c. Explain stop and wait automatic repeat request for noisy channel. **(08 Marks)**

d. Perform bit stuffing on the given bit stream
0001111111001111101000 assume flag as 01111110. **(02 Marks)**

3 a. A pure ALOHA network transmits 200 bit frames on a shared channel of 200kbps. What is the throughput if system produces: i) 1000 frames per second; ii) 500 frames per second. **(04 Marks)**

b. Explain 1-persistent, non-persistent and p-persistent with flow diagram. **(06 Marks)**

c. With suitable diagram and example explain CDMA. **(06 Marks)**

d. Explain polling as a controlled access technique. **(04 Marks)**

4 a. Explain frame format of 802.3 MAC frame. **(06 Marks)**

b. Define the type of the following destination address and justify answer:
i) 4A : 30 : 10 : 21 : 10 : 1A ii) 47 : 20 : 1B : 2E : 08 : EE. **(04 Marks)**

c. Explain bridge Ethernet, switched Ethernet, full duplex Ethernet. **(10 Marks)**

PART – B

5 a. Explain what is loop problem and solution for a loop problem in a bridge with suitable examples and diagrams. **(10 Marks)**

b. Explain bus backbone and star backbone networks. **(06 Marks)**

c. What is VLAN? Explain briefly. **(04 Marks)**

6 a. What is NAT? Explain how NAT help in address depletion. **(05 Marks)**

b. Explain IPV4 datagram. **(05 Marks)**

c. An ISP granted a block of addressing with 190.100.0.0/16. The ISP needs to distribute these address to three groups of customer as follows:
i) First group has 64 customers each with 256 addresses.
ii) Second group has 128 customers each with 128 addresses. **(05 Marks)**

d. Explain class full addressing for IP address. **(05 Marks)**

7	a.	With suitable diagram explain distance vector routing.	**(10 Marks)**
	b.	Explain different solution to two-node instability.	**(05 Marks)**
	c.	Explain source-based tree and group shared based tree.	**(05 Marks)**
8	a.	Describe a TCP connection establishment using three way handshake.	**(10 Marks)**
	b.	Explain TCP and UDP datagram.	**(10 Marks)**

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10EC/TE72

Seventh Semester B.E. Degree Examination, June/July 2014

Optical Fiber Communication

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. List the advantages, disadvantages and applications of optical fiber communication system. **(08 Marks)**

b. A step index multimode fiber with a NA of 0.2 supports approximately 1000 modes at an 850 nm wavelength. What is the diameter of its core? How many modes does the fiber support at 1320 nm and at 1550 nm? **(09 Marks)**

c. Define acceptance angle and critical angle. **(03 Marks)**

2 a. Explain macro bending and micro bending losses with a neat diagram. **(10 Marks)**

b. Explain the signal distortion in fibers. **(06 Marks)**

c. Write a note on: i) Attenuation, ii) Absorption. **(04 Marks)**

3 a. List the desirable characteristics of the LED and LASER diode as optical sources. **(08 Marks)**

b. Explain p-i-n photodiode with a neat diagram. **(08 Marks)**

c. Photons of energy 1.53 × -19 J are incident on a photodiode which has responsibility of 0.65 A/W. If the optical power level is 10 μW, find the photo current gencrated. **(04 Marks)**

4 a. What is splicing? Explain the fusion splicing with a neat diagram. **(08 Marks)**

b. List the requirements of a good connector. **(06 Marks)**

c. Explain the fundamental types of misalignments between fibres. **(06 Marks)**

PART – B

5 a. With a neat block diagram explain the digital signal transmission through an optical data link. **(12 Marks)**

b. Give the classification of front end amplifier used in optical fiber communication system. Explain any one of them. **(08 Marks)**

6 a. Explain the optical power loss model with a neat diagram. **(10 Marks)**

b. Clearly explain the analog link with the major noise contributions at each stage. **(10 Marks)**

7 a. What is WDM? Briefly explain the advantages of WDM. **(04 Marks)**

b. Explain the polarization independent isolator with a neat diagram. **(08 Marks)**

c. Write a note on MEMS technology. **(08 Marks)**

8 a. What are salient features of semiconductor optical amplifiers? **(06 Marks)**

b. Write notes on:
i) SONET/SDH rings
ii) High speed light waveguide **(14 Marks)**

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10EC73

Seventh Semester B.E. Degree Examination, June / July 2014
Power Electronics

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. With the help of a block diagram, explain the working of a converter system. Also explain how thyristor converters are classified. **(07 Marks)**

b. Give symbol, characteristic features of the following devices: i) GTO ii) TRIAC iii) MOSFET iv) DIAC. **(08 Marks)**

c. What are the peripheral effects caused by power electronic converters? What are the remedies for them? **(05 Marks)**

2 a. In the circuit of Fig. Q2 (a), the BJT is specified to have β in the range of 8 to 40. If V_{CC} = 200 V, R_C = 11 Ω, V_B = 10 V, $V_{CE(sat)}$ = 1 V and $V_{BE(sat)}$ = 1.5 V. Find (i) the value of R_B that results in saturation with an ODF of 5, (ii) the forced β_f and (iii) the power loss P_T in the transistor. **(09 Marks)**

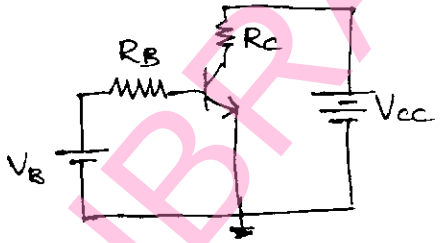

Fig. Q2 (a)

b. State and explain the output and transient characteristics of enhancement type MOSFET. **(08 Marks)**

c. Compare IGBT and MOSFET as switching devices. **(03 Marks)**

3 a. Explain the dynamic characteristics of SCR during turn on and turn off with suitable waveforms. **(08 Marks)**

b. In the thyristor circuit shown in Fig. Q3 (b), the SCR has a latching current of 50 mA and is fired by a pulse of length 50 μ sec. Show that without the resistor R, the thyristor will fail to remain on when the firing pulse ends and then find the maximum value of R to ensure firing. **(04 Marks)**

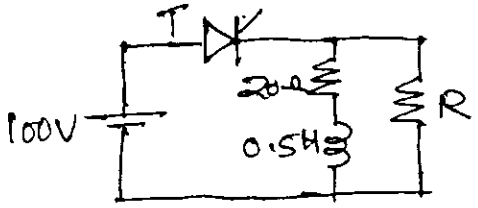

Fig. Q3 (b)

c. Explain the need for $\frac{dv}{dt}$ and $\frac{di}{dt}$ protection. A SCR circuit has the following data: Supply voltage = 200 V, $\frac{dv}{dt}$ rating = 100 V/μs, $\frac{di}{dt}$ rating = 50 A/μsec. Calculate the snubber circuit elements using approximate expressions. **(08 Marks)**

4 a. What will be the average power in the load for the halfwave controlled rectifier circuit shown in Fig. Q4 (a), when $\alpha = \frac{\pi}{4}$. Assume the SCR to be ideal. Supply voltage is $330\sin 314t$. Also calculate the RMS power and the rectification efficiency. **(10 Marks)**

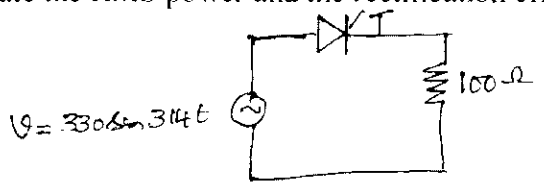

Fig. Q4 (a)

b. With the help of a neat circuit diagram and relevant waveforms. explain the working of a single phase dual converter with inductive load. **(10 Marks)**

PART – B

5 a. Calculate the conduction time of SCR and the peak SCR current that flows in the circuit shown in Fig. Q5 (a) employing self commutation if the supply voltage is 300 V. C = 1 μf, L = 5 mH and R_L = 100 Ω. Assume that the circuit is initially relaxed. **(08 Marks)**

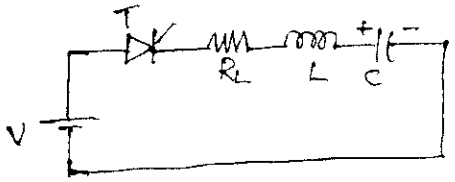

Fig. Q5 (a)

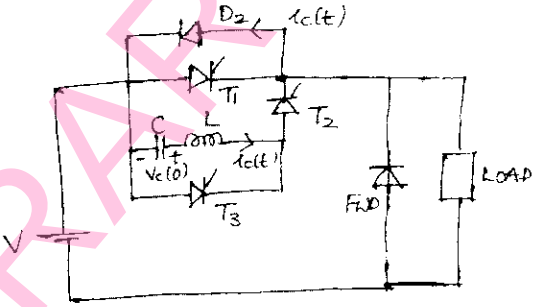

Fig. Q5 (b)

b. Fig. Q5 (b) shows a resonant pulse commutation circuit with the accelerating diode D_2 connected across the thyristor T_2. The initial capacitor voltage $V_c(0)$ = 200 V, C = 30 μf and L = 3 μH. Determine the circuit turn off time t_c, if the load current is I_L = 200 A. **(12 Marks)**

6 a. With the help of a neat circuit diagram and the relevant waveforms, explain the working of a single phase AC voltage controller with RL load. Derive an expression for the RMS output voltage. **(10 Marks)**

b. Find the RMS and average current flowing through the heater shown in Fig. Q6 (b). The delay angle of both the thyristors is 45°. **(10 Marks)**

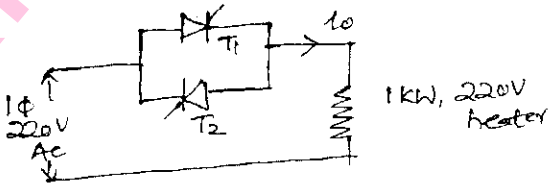

Fig. Q6 (b)

7 a. Derive an expression for the peak to peak ripple current ΔI for a stepdown chopper with RL load. **(10 Marks)**

b. What is a switching mode regulator? With the help of circuit diagrams and waveforms. explain the working of a Boost regulator with continuous current i_L. **(10 Marks)**

8 a. Explain the principle of operation of a single phase full bridge inverter with suitable circuit diagram and waveforms. **(10 Marks)**

b. Explain briefly the various voltage control techniques in single phase inverters. **(10 Marks)**

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10EC74

Seventh Semester B.E. Degree Examination, June/July 2014

Embedded System Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. What is an embedded system? What is the purpose of a watchdog timer in an embedded application? **(05 Marks)**

b. Briefly describe the major elements of the embedded system development life cycle. **(06 Marks)**

c. Explain the implementation of a microprocessor based embedded system. **(05 Marks)**

d. What is the difference between hard, firm and soft real time system? **(04 Marks)**

2 a. Explain the block diagram of a digital signal processor. **(05 Marks)**

b. Draw and explain the architecture of the data path and the memory interface for a simple microprocessor at the register transfer level. **(06 Marks)**

c. What is meant by the array of an instruction? Explain the terms one, two, three operand instruction. **(04 Marks)**

d. What do you mean by addressing mode? What are different instructions in an instruction set view? **(05 Marks)**

3 a. Discuss the benefits of using SRAM versus DRAM. In what kind of embedded system applications should the following types of ROM used: ROM, PROM, EEPROM, FLASH? **(06 Marks)**

b. Explain the direct mapping cache management strategy with an example. What are the trade off between write through and delayed write algorithm? **(08 Marks)**

c. A microprocessor based system has 8 address lines and 8 data lines requires an SRAM system that can store up to 4K 16 bit words. But largest available memory device is 1K × 8. Design memory system that supports above said data. **(06 Marks)**

4 a. Briefly explain waterfall, V cycle, spiral life cycle models. **(10 Marks)**

b. What are the general software design steps? Explain the hardware architecture of the counter in designing a counter system. **(10 Marks)**

PART – B

5 a. Explain the different functions of embedded operating system. **(10 Marks)**

b. What is a task control block? What are some of the major components of task control block? **(05 Marks)**

c. Explain the time management system of real time operating system. **(05 Marks)**

6 a. Explain the operating system architecture. **(05 Marks)**

b. Briefly explain the state transitions in the task control block module system. **(05 Marks)**

c. What is a foreground/background system? What is the difference between a foreground and a background task? **(05 Marks)**

d. What is context switching? Describe the sequence of steps that are necessary to handle an occurrence of an interrupt. **(05 Marks)**

7 a. Describe the methods by which we can perform a time loading analysis of an embedded a time loading analysis of an embedded application. Discuss the advantages and disadvantages of each. **(10 Marks)**

b. Analyze the algorithm given below that accepts as I/P an array of integer and the number of elements in the array. Obtain complexity function for the algorithm.

```
int total (int myArray[ ] , int n)
{
   int sum = 0;
   int  i = 0;
   For (i = 0; i < n; i++)
   {
     sum = sum + myArray[i];
   }
   return sum;
}
```

(10 Marks)

8 a. Explain the difference between linear, quadratic, logarithmic and exponential growth with respective to a software algorithm. **(10 Marks)**

b. Analyse the following two types of loop:

i) Determine the number of iterations to be performed.

ii) Determine the number of steps per iteration of total time.

loop 1	loop 2
int sum = 0;	int sum = 0;
For (int j = 0; j < N; j++)	For (int j = 0; j < 100; j++)
sum = sum + j;	sum = sum + j;

(10 Marks)

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Seventh Semester B.E. Degree Examination, June/July 2014
DSP Algorithms and Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. What is Digital Signal Processing? Explain the issues to be considered in designing and implementing a DSP system. **(09 Marks)**

b. Write a MATLAB code for design an FIR filter using Parks-McClellen method. **(05 Marks)**

c. Explain the decimation and interpolation processes with an example. **(06 Marks)**

2 a. What is role of a shifter in DSP? Explain the implementation of 4-bit shift right barrel shifter with a diagram. **(06 Marks)**

b. Identify the addressing modes of the operands in each of the following instructions and their operation:
(i) ADD B (ii) ADD 5678h (iii) ADD + *addrreg (iv) ADD *addrreg, offsetreg – **(08 Marks)**

c. Explain the purpose of a program sequencer with a block diagram. **(06 Marks)**

3 a. Describe the multiplier / adder unit of TMS320C54× processor with a neat block diagram. **(06 Marks)**

b. Describe any four data addressing modes of TMS320C54XX DSP with examples **(08 Marks)**

c. Assuming current contents of AR_3 to be 200h, what will be its contents after each of the following TMS320C54× addressing modes is used? Assume that the contents of AR0 are 20h.
(i) $*AR_3$ +0 (ii) $*AR_3$ + (iii) $*+AR_3(40h)$ **(06 Marks)**

4 a. Describe the operation of the following instructions of TMS320C54× processor with an example :
(i) MAC (ii) RPT (iii) MPY **(06 Marks)**

b. Write a program to find the sum of a series of signed numbers stored at successive locations in the data memory and place the result in the accumulator A

ie., $A = \sum_{i=410h}^{41fh} dmad(i)$ **(06 Marks)**

c. Describe the operation of hardware timer with a neat diagram. **(08 Marks)**

PART – B

5 a. Describe the importance of Q-notation in DSP algorithm implementation, with examples.

b. What are the values represented by 16-bit fixed point number N – 4000h in Q15, Q10, Q7 notations? **(10 Marks)**

c. Explain how the FIR filter algorithms can be implemented using TMS320C54XX processor. **(10 Marks)**

6 a. Explain a general DITFFT butterfly in place computation structure. **(04 Marks)**

b. Determine the no. of stages and number of butterflies in each stage and the total number of butterflies needed for the entire computation of 512 point FFT. **(06 Marks)**

c. Explain how the bit-reserved index generation can be done in 8-point FFT. Also write a TMS320C54XX program for 8-point DITFFT bit reversed index generation. **(10 Marks)**

7 a. Explain the memory interface block diagram for the TMS320C54XX processor. **(06 Marks)**

b. Draw the I/O interface timing diagram for read-write-read sequence of operation. **(06 Marks)**

c. What are interrupts? How interrupts are handled by the C54XX DSP processors. **(08 Marks)**

8 a. Draw the block diagram of PCM3002 CODEC and explain about it. **(10 Marks)**

b. With the help of block diagram, explain the image compression and reconstruction using JPEG encoder and decoder. **(10 Marks)**

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10EC762

Seventh Semester B.E. Degree Examination, June/July 2014
Real Time Systems

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Define real time system. Explain the different classifications with example. **(10 Marks)**

b. Explain computer control system with a suitable diagram. **(06 Marks)**

c. Write any four responsibilities of a control engineer. **(04 Marks)**

2 a. What is DDC? What are the advantages of DDC over analog control? Discuss PID control algorithm. **(10 Marks)**

b. Explain the following: i) Supervisory control system; ii) Batch process and continuous process. **(10 Marks)**

3 a. Explain the ISO seven layer model for data communication. **(10 Marks)**

b. Mention the features of specialized processors and explain SIMD and MIMD with a neat diagram. **(10 Marks)**

4 a. Explain simple table-driven approach used for application oriented software. **(10 Marks)**

b. Define the following with respect to real time programming:
i) Scope and visibility.
ii) Global and local variables.
iii) Modularity.
iv) Data types. **(10 Marks)**

PART – B

5 a. With a neat block diagram, explain the typical structure of RTOS. **(10 Marks)**

b. What is tack management? List the functions of task management. With a neat diagram discuss different states. **(10 Marks)**

6 a. Explain with a suitable diagram the multi-user and multi-tasking operating systems. **(10 Marks)**

b. What are the two scheduling strategies? Explain briefly. **(10 Marks)**

7 a. Explain the different phasor involved in the design of a RTS. **(10 Marks)**

b. Explain software design for RTS using software module. **(10 Marks)**

8 a. With a general arrangement for drying overn, explain its requirements. **(10 Marks)**

b. Write short notes on: i) Software modeling; ii) Yourdon methodology. **(10 Marks)**

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